WHAT IS CLAIMED IS:

1. A layout of a nonvolatile memory structure, comprising:

a plurality of memory array banks; and

a plurality of double-ended sense amplifiers,

wherein each of the double-ended sense amplifiers is implemented between two of the memory array banks for sharing use, wherein when one array bank is decoded, the other one array bank serving as a reference array.

2. The layout of the nonvolatile memory structure according to claim 1, wherein every two of the memory array banks are grouped in one dual bank, and one of the double-ended sense amplifiers is implemented in the dual bank.

3. The layout of the nonvolatile memory structure according to claim 1, wherein a predetermined number of the memory array banks are grouped into one bank unit for multiple bank units, and one of the double-ended sense amplifiers is implemented between two of the bank units.

4. A memory array bank structure for a nonvolatile memory, comprising:

a plurality of memory cell transistors are arranged in a matrix form by a plurality of rows and a plurality of columns, wherein the rows are corresponding to word lines and at least two adjacent columns are grouped into a multi-cell column with respect to one bit line, the bit line is branched into multiple branch bit lines, at least including a first branch bit line selected by a first selection signal and a second branch bit line selected by a second selection signal, wherein the first branch bit line connects all drain electrodes at one side of the multi-cell column and the second branch bit line connects

all drain electrodes at the other side of the multi-cell column, and one common source line connected all source electrodes of the multi-cell column;

a selection reference row of transistors with respect to the multi-cell columns coupled to one of the world lines as a reference word line, wherein gate electrodes of the transistors in the selection reference row are coupled to a selection reference signal, a first source/drain electrode of the transistors is coupled to the first branch bit line, and a second source/drain electrode of the transistors is coupled to the common source line of the next multi-cell column; and

a plurality of selection transistors coupled to the multi-cell columns at the common source lines, respectively, in which a bank selection signal can be fed.

5. The memory array bank structure according to claim 4, wherein the transistors of the selection reference row has a relatively large channel length.

6. A memory array bank structure for a nonvolatile memory, comprising:

a plurality of first column of memory cells coupled in cascade as a first column, having a first end side and a second end side;

a plurality of second column of memory cells coupled in cascade as a second column, having a first end side and a second end side, wherein the first column and the second column are arranged to has a plurality of rows indicated as word lines;

a first selection transistor coupled in series with the first end side of the first column of memory cells;

a second selection transistor coupled in series with the second end side of the second column of memory cells;

a bit line, which has a first branch bit line and a second branch bit line, respectively coupled to the first column and the second column via the first selection transistor and the second selection transistor; and

a word line reference cell row of reference cell transistors, wherein the reference cell transistors are respectively coupled to the first column and the second column at the second ends in series,

wherein the open ends of the first branch bit line and the second branch bit line are coupled to a double-ended sense amplifier.

7. The memory array bank structure according to claim 6, wherein the nonvolatile memory comprises a NOR flash memory or a DiNOR flash memory.

8. The memory array bank structure according to claim 6, wherein each of the reference cell transistors has large channel length.

9. A cell layout for a nonvolatile memory, comprising:

a first memory bank, having

a bank selection transistor row at one side and a reference cell row at the other side, wherein two adjacent columns are grouped into one sector with two bit lines, and rows are arranged to be word lines;

a second memory bank, having

a bank selection transistor row at one side and a reference cell row at the other side, wherein two adjacent columns are grouped into one sector with two bit lines and rows are arranged to be word lines, wherein the bit lines of the first memory bank and the second memory bank are correspondingly connected together, as well as the first memory bank

and the second memory bank are coupled at the sides having the bank selection transistor row; and

a plurality of double-ended sense amplifiers, wherein each one of the sense amplifier is implemented between the two adjacent bit lines.

10. The cell layout according to claim 9, wherein the reference cell row includes transistors with relatively large channel length but same gate level.

11. The cell layout according to claim 9, wherein the nonvolatile memory includes a folded bit line structure.

12. A cell layout for a nonvolatile memory, comprising:

a first memory bank, having

a bank selection transistor row at one side and a reference cell row at the other side, wherein two adjacent columns are grouped into one sector with two branch bit lines, the two branch bit lines are combined into one bit line in the bank selection transistor row and rows are arranged to be word lines;

a second memory bank, having

a bank selection transistor row at one side and a reference cell row at the other side, wherein two adjacent columns are grouped into one sector with two branch bit lines, the two branch bit lines are combined into one bit line in the bank selection transistor row and rows are arranged to be word lines; and

a plurality of double-ended sense amplifiers, wherein each one of the sense amplifier is implemented to receive the two bit lines respectively from the first memory bank and the second memory bank.

13. The cell layout according to claim 12, wherein the nonvolatile memory includes an open bit line structure.

14. The cell layout according to claim 12, wherein the reference cell row includes transistors with relatively large channel length but same gate level.

15. A via-mask read only memory (ROM) layout structure, comprising:

a dynamic random access memory (DRAM) like layout structure, as a main body structure, including an array of coding transistors;

a grounding structure line over source regions of the coding transistors, wherein the grounding layer is located at a position, where capacitor areas are defined in a DRAM structure; and

a plurality of vias with respect to a portion of the coding transistors, for coupling the source regions with the grounding structure line, wherein each of the vias in the corresponding coding transistors represents a first binary data, and the coding transistors without the vias represent a second binary data.

16. The via-mask ROM layout structure of claim 15, wherein the first binary data is "1" and the second binary data is "0".

17. The via-mask ROM layout structure of claim 15, wherein the first binary data is "0" and the second binary data is "1".